Towards Selective Cobalt Atomic Layer Deposition for Chip-to-Wafer 3D Heterogeneous Integration

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***Abstract*— The feasibility of a 3D bonding technology for ultra-dense input/output (I/O) interconnects using cobalt selective atomic layer deposition (Co ALD) is explored with a preliminary testbed. Steady-state thermal simulations benchmark the Co ALD bonding technology to investigate the potential thermal benefits compared to conventional bonding technologies such as microbumps (µ-bumps) and hybrid bonds. Preliminary testbeds containing horizontal Cu/100 nm Gap/Cu structures are fabricated to show the feasibility of using Co ALD as a high-density Cu-Cu interconnect bonding technology. SEM and XPS are used to characterize the test structures, showing that after 400 cycles of Co ALD deposition, the 100 nm gap is filled between the aligned Cu pads.**

***Keywords*—Selective cobalt ALD, chiplets, 3D heterogeneous integration**

I. Introduction

To meet the demands of data-intensive applications such as artificial intelligence (AI) and high-performance computing (HPC), there is a need for tighter integration to minimize electrical interconnect delays and energy. Unfortunately, there is a slowdown in traditional device scaling for nanoscale CMOS technology as on-chip interconnect parasitics are becoming more dominant with device scaling. Therefore, there is a growing interest in 3D heterogeneous integration technologies as demonstrated by TSMC's SoIC [1] and AMD's 3D V-Cache [2] technologies. 3D heterogeneous integration technologies have the potential for high-density interconnects, bandwidth, and low-power consumption [3], but there are limitations in bonding technologies due to materials and small dimensions which can create challenges. For example, µ-bumps have been fabricated with a reflow or thermocompression process, however, as their pitch scales down, the under-bump metallization (UBM) thickness starts to become a bottleneck [4-5].

Typical I/O pitches for µ-bumps range from hundreds of µm to ~50 µm for conventional flip chip stacking [6], therefore limiting the number of I/O's. Scaling µ-bumps to less than 30 µm can cause adjacent interconnects to short during bonding and can also decrease the thermomechanical stability due to the creation of unfavorable intermetallic compounds [7]. This has led to the exploration of new bonding technologies to further drive interconnect scaling below 10 µm. Cu-Cu direct bonding methods such as surface activated bonding [8] and Cu passivation methods [9] have been explored. However, these methods require relatively high temperatures, large mechanical forces, and controlled surface cleanliness and planarity. Hybrid bonding has been demonstrated at sub-10 µm pitch in an industry product [2] and below sub-micron in industry [10], but this bonding process requires extreme surface cleanliness and chemical mechanical polishing (CMP) [11] as inappropriate dishing on the Cu surfaces can lead to bonding failure, making die-to-wafer bonding challenging [12].

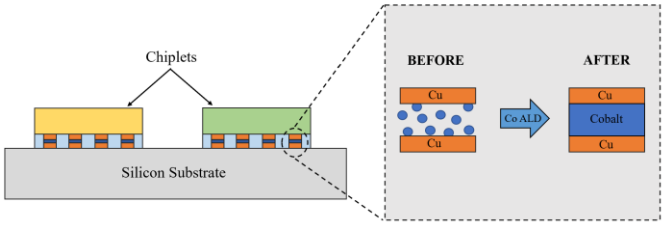

Fig. 1: ALD bonding concept.

In this work, first we present a thermal study to investigate the benefits of selective Co ALD bonding technology [13] relative to current state of the art µ-bumps and hybrid bonds. Following the thermal analysis, we will also report the experimental results of testbeds containing Cu/Gap/Cu horizontal test structures with the gap size of 100 nm and pitches ranging from 1 µm– 10 µm. The results show the feasibility of using selective Co ALD for high-density Cu-Cu interconnect bonding. SEM, EDAX, and XPS are used to characterize the testbed before and after Co deposition and to measure the selectivity of Co ALD on the Cu and Si_3N_4 substrate. Compared to thermocompression bonding technologies such as Cu-Cu direct bonding or hybrid bonding, the Co ALD chip-to-wafer bonding process deposits an intermediate layer between the Cu pads and therefore does not require metal diffusion to create the bond. This process also does not require an external mechanical force, extreme chemical mechanical polishing, and surface cleanliness. In addition, the Co ALD process has exceptional film thickness controllability at the Angstrom range with I/O pads that have various diameters and pitches. These attributes suggest that this bonding technology has the potential to aggressively shrink the Cu I/O pitch to sub-micron.

The paper is divided into the following: In Section II, a thermal model of a TSV-based memory on CPU 3D design is

used to benchmark the Co ALD bonding technology to µ-bumps and hybrid bonds. In Section III, we show the experimental results of horizontal test structures with a gap size of 100 nm and pitches varying from 1 µm – 10 µm, followed by the conclusion.

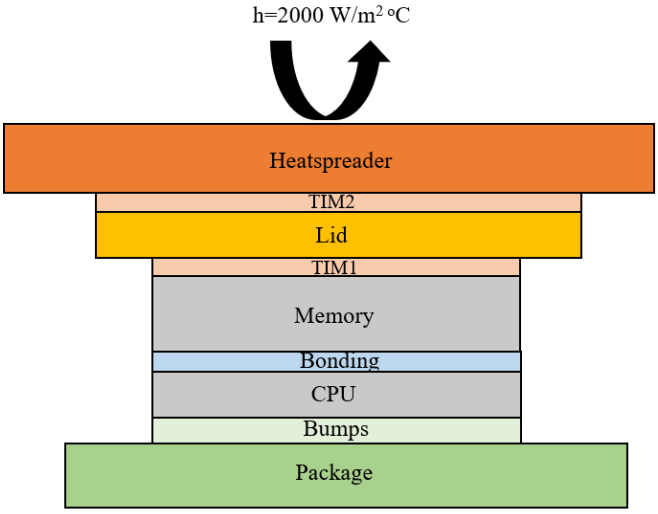

Fig. 2: Cross-section of TSV-based memory on CPU 3D design

TABLE I
EXPERIMENTAL SETUP

Parameter (x,y,z)	Value
Heatspreader	23.6 mm x 25.07 mm x 1 mm
TIM2	13.6 mm x 15.07 mm x 30 µm
Lid	13.6 mm x 15.07 mm x 1 mm
TIM1	8.6 mm x 10.07 mm x 30 µm
Memory	8.6 mm x 10.07 mm x 635 µm 8.6 mm x 10.07 mm x 7 µm
Bonding	8.6 mm x 10.07 mm x 25 µm 8.6 mm x 10.07 mm x 3 µm
CPU	8.6 mm x 10.07 mm x 50 µm 8.6 mm x 10.07 mm x 7 µm
Bumps	8.6 mm x 10.07 mm x 50 µm
Package	18.6 mm x 20.07 mm x 1 mm
Heat transfer coefficient (h)	2000 W/m² °C (air)
Ambient Temperature	33 °C
Total Power	CPU: 10.8 W, Memory: 1.5 W

II. Thermal Model

A TSV-based 2-tier 3D design described in Fig. 2 is evaluated to benchmark Co ALD bonds against conventional µ-bumps and hybrid bonds for steady-state in Ansys Mechanical (ver. 2021 R1). We assume a memory on CPU stack where C4 bumps are uniformly distributed throughout the bumps tier and the CPU and memory die are connected through a bonding tier that can be µ-bumps, hybrid bonds, or Co ALD bonds. Finally, we attach a copper lid and copper heat spreader with a thermal interface material (TIM) to the die stack and assume a heat transfer coefficient of 2000 W/m² °C. The memory tier dissipates a uniform power, and the CPU tier is designed after an 8-core CPU based on [14]. For the CPU core design, a 50 µm x 50 µm resolution power map is generated with localized hotspots reaching up to 16 W/mm² to emulate a CPU design. We assume 1 core is activated while the other 7 cores are idle. Table I describes the parameters assumed for the simulations.

A. Hybrid Bonds & Co ALD Bonds Unit Models

As the bonds are distributed uniformly throughout the bonding tier, this can result in hundreds of interconnects. Therefore, to reduce the complexity of the model while not sacrificing the accuracy, a unit model approach described in [15] was used to extract the effective thermal conductivity of the bonding tier for hybrid bonds and Co ALD bonds.

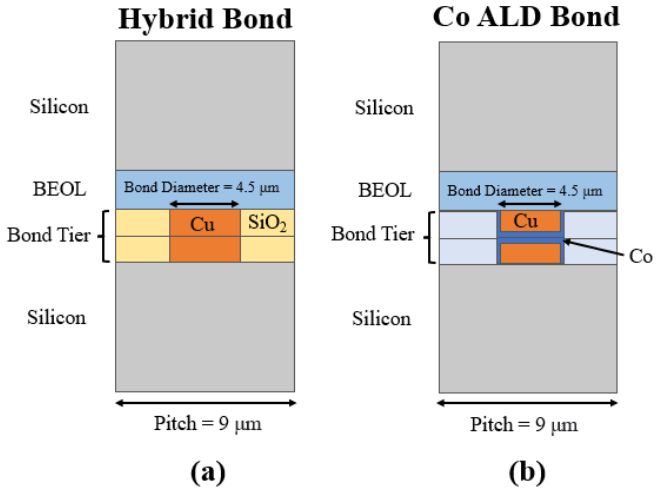

Fig. 3: Unit model of (a) hybrid bond and (b) Co ALD bond

For comparison, hybrid bonds and Co ALD bonds have a pitch of 9 µm, as demonstrated in [2], and bond diameter of 4.5 µm (Fig. 3). For the Co ALD bonds, 100 nm of Co is assumed to bond the two copper pads. As Co ALD bonds are not restricted to low thermal conductivity 'underfill' such as SiO_2, we assume the dielectric surrounding the bonds to be a high conductivity material.

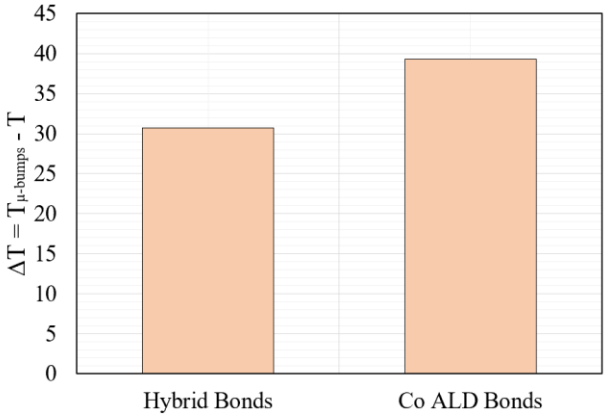

Fig. 4: Increase in maximum junction temperature for CPU tier for different bonding configurations.

B. Steady-State Benchmarking

Three bonding configurations were considered for the TSV-based 2-tier 3D design: 1) µ-bumps; 2) hybrid bonds; and 3) Co ALD bonds. Fig. 4 presents $\Delta T_{j,max,core}$ relative to the µ-bump baseline for hybrid bonds and Co ALD bonds. It can be seen that the two bonding configurations have a lower temperature compared to µ-bumps due to the decreased thermal resistance of the stack. However, Co ALD bonds result in a lower temperature compared to hybrid bonds due to the high thermal conductivity material surrounding the bonds. This leads to

better heat spreading between the CPU tier to the heat spreader, demonstrating the potential thermal benefits of Co ALD bonds.

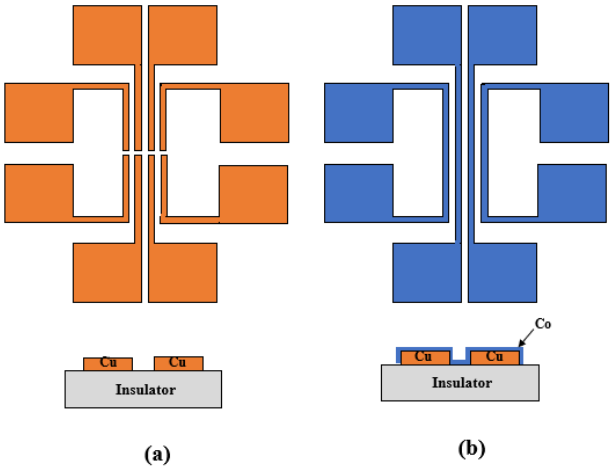

Fig. 5: Schematic of Co ALD lateral testbed design concept. (a) Before Co ALD deposition, the Cu pads are in open circuit. (b) After Co ALD deposition, the Cu pads form a short circuit.

III. Cu/Gap/Cu Lateral Testbed

To demonstrate the Co ALD bonding technology, we introduce a Cu/Gap/Cu lateral testbed that is fabricated to enable an air-gap size of 100 nm and pitches from 1 µm – 10 µm. The testbed, described in Fig. 5 includes fine pitch gap structures and misalignment structures.

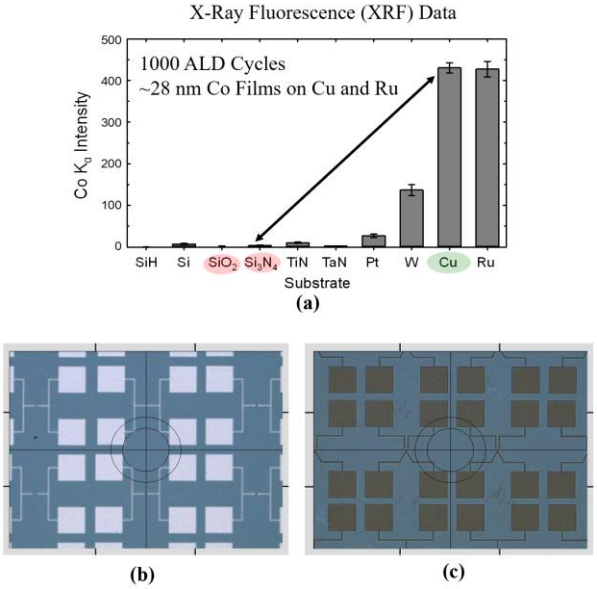

Fig. 6: Schematic of Co ALD lateral testbed design concept. (a) Before Co ALD deposition, the Cu pads are in open circuit. (b) After Co ALD deposition, the Cu pads form a short circuit.

A. Fabrication

First, electron beam lithography (EBL) is used to fabricate the small gap sizes, then 10 nm/40 nm of Ti/Cu is deposited on an insulating material, such as Si_3N_4, using a PVD lift-off process. Probing pads are then fabricated to test that the Cu pads are in an open circuit before deposition and a closed circuit after deposition. The bonding pads range from 500 nm – 5 µm to enable pitch sizes from 1 µm – 10 µm.

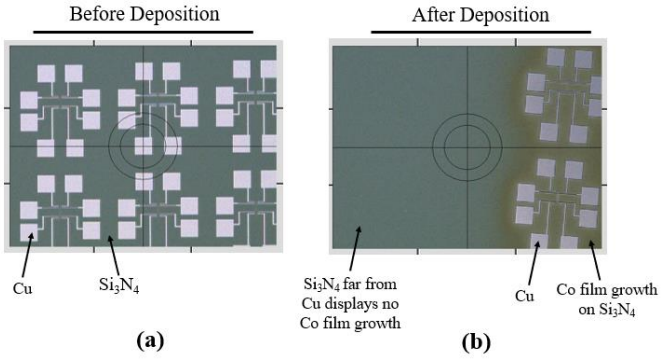

Fig. 7: Lateral testbed as fabricated (a) before Co ALD deposition and (b) after deposition Co ALD deposition.

B. Results

Initially, the following ALD process is used for the testbed: $Co(thd)_2$ (3.5 s)/N_2 purge (10 s) /1,1- dimenthylhydrazine (0.2 s)/N_2 purge (10 s) at 285 ºC. This cycle is repeated until the gap between the two pads is filled. The sample is then annealed at 350 ºC to remove nitrogen content from the films to produce high purity Co metal. The growth rate of each cycle is ~0.3 Å. In Fig. 6, a simple, copper pattern that required a single lift-off was deposited on Si_3N_4 to show that this process is selective on metallic versus insulating materials.

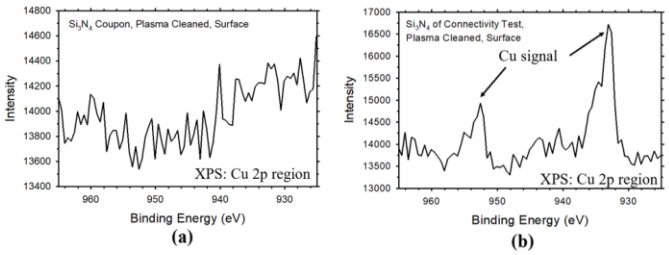

Fig. 8: XPS Cu 2p surface scans of (a) Si_3N_4substrate coupon without Cu contamination and (b) the Si_3N_4 surface of a testbed displaying Cu contamination.

However, in Fig. 7, it can be seen that after 1000 ALD cycles that there is no cobalt film growth on the Si_3N_4 far from the Cu/Gap/Cu lateral testbeds but near the Cu testbeds, there is Co growth on the Si_3N_4, and poor selectivity can be observed.

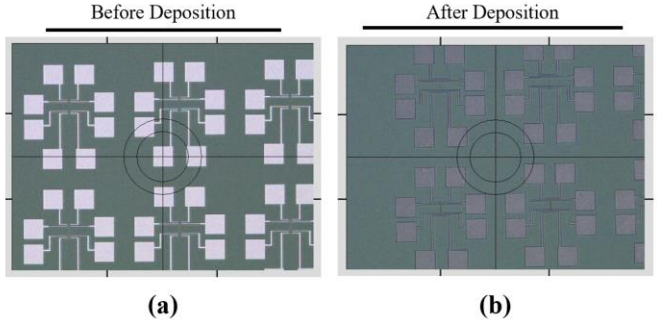

Fig. 9: Lateral testbed treated with 7-minute acetic acid wet etch (a) before deposition and (b) after deposition.

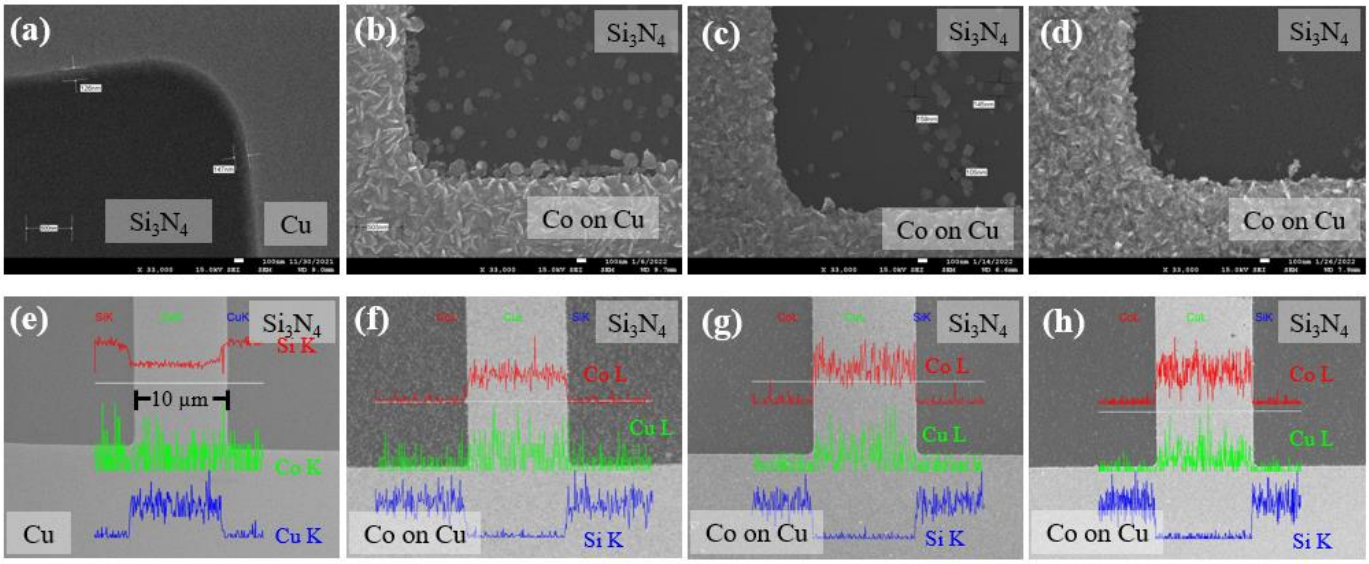

Figure 10: SEM of Co etched with 10% formic acid (a) before deposition, (b) after deposition (c) after a 1 minute etch with 10% formic acid, and (d) after a 2 minute etch with 10% formic acid. EDAX line scans (e) before deposition, (f) after deposition, (g) after a 1 minute etch with 10% formic acid, and (h) after a 2 minute etch with 10% formic acid.

This was found to be due to Cu contamination on the Si_3N_4 around the Cu testbeds. In Fig. 8, XPS was used to compare the Cu signal on Si_3N_4 when there is no Cu deposited versus on the lateral testbed demonstrating how around 1% of Cu contamination on the Si_3N_4 substrate is sufficient for Co nucleation and film. Based on experimental evidence, we found that the 2-minute O_2 plasma clean process potentially caused the Cu contamination around the Cu testbeds. This is possibly due to the prolonged plasma cleaning may have caused surface re-deposition of Cu [16].

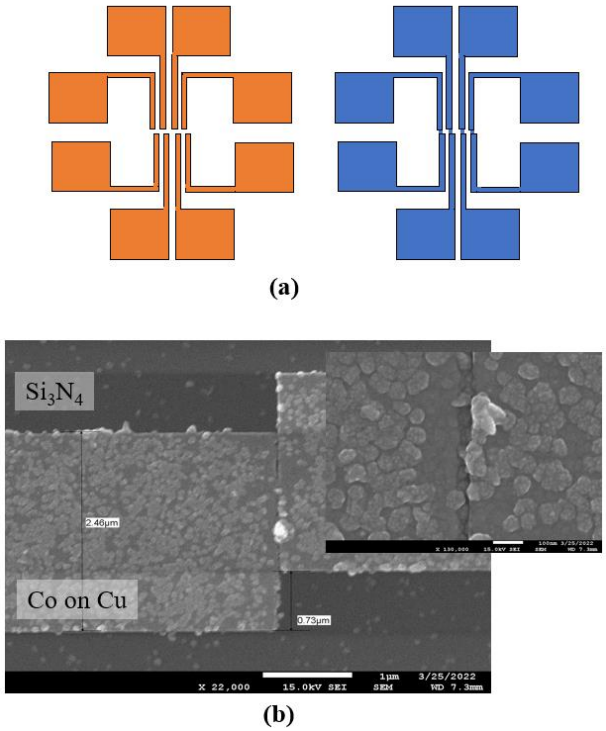

Fig. 11: 100 nm misaligned testbed (a) concept and (b) SEM image after Co deposition forming a Cu-Co-Cu bridge.

Therefore, to improve the selectivity, the testbed was treated with a seven-minute ~99% glacial acetic acid wet etch at room temperature prior to deposition. In Fig. 9, it can be seen that the pre-treatment helped remove the Cu contamination around the Cu testbeds, resulting in improved selectivity. In addition, a post-deposition treatment of 10% formic acid wet etch for up to 2-minutes at room temperature was done on Cu samples with no Cu contamination to help further improve the selectivity of the Co ALD deposition. In Fig. 10, SEM and EDAX indicate that the 10% formic acid wet etch, performed here for up to 2 minutes, is an effective way to remove undesired cobalt growth. These pre- and post-deposition treatments prove to be an effective method to improve the selectivity of the Co ALD process by removing the Cu contamination around the testbeds and removing the excessive Co growth.

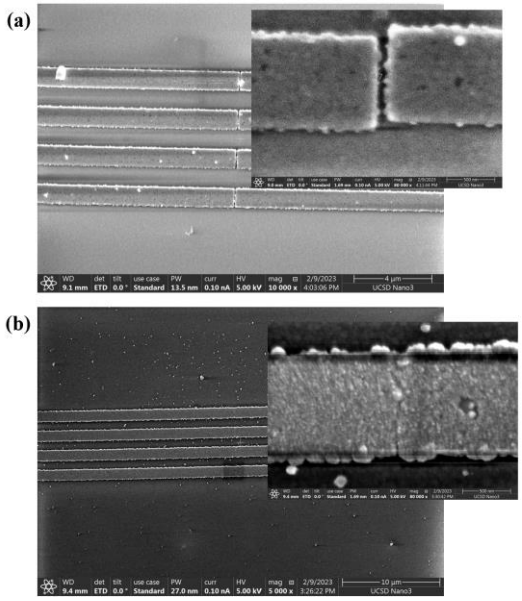

Fig. 12: SEM image of Cu pads (a) before deposition and (b) after 400 cycles of Co ALD deposition using $Co(DAD)_2$ + TBA at 190ºC.

In Fig. 11, an SEM image shows Co on the Cu bond pad, forming a Cu-Co-Cu bridge across a 100 nm gap using $Co(thd)_2$. Although there are small island growths, as observed on the Si_3N_4 substrate, the Co is discontinuous and electrically isolated. To further improve the selectivity of the Co deposition and reduce Cu contamination on the testbed, the Cu pads were completed with a single lift-off step that did not require an O_2 plasma clean.

The Co ALD recipe was also optimized to improve the quality of the Co film growth. The following ALD process conditions were used to improve the Co ALD recipe: $Co(DAD)_2$ + TBA (tertiary butyl amine) 8x (1 s fill/1 s wait/1 s dose/1 s wait) + 50 s pump out. TBA: 13 ms + 25 s pump out, 190 ^oC. The growth rate is about 1.6 Å per cycle.

Fig. 12(a) is an SEM image of the copper pads separated by a 100 nm air-gap before deposition. In Fig. 12(b), it can be seen that the 100 nm air-gap between the Cu pads is closed after 400 cycles of Co ALD without causing the adjacent copper pads to short with each other. The deposited Co film and selectivity improved after optimizing the Co ALD recipe and reducing the Cu contamination around the Cu structures. Furthermore, the Co growth on the insulator substrate are small growths that are electrically isolated.

This proposed method is not limited to Co and can potentially be compatible with any thermal ALD deposition with high selectivity on metal substrates. Compared to other thermocompression bonding technologies such as Cu-Cu direct bonding or hybrid bonding, ALD bonding does not require metal diffusion to create the bond between the Cu pads. Instead, the ALD process deposits an intermediate layer that does not require a mechanical force or high temperature. In addition, ALD can control the film growth at the sub-nanometer level on I/O pads with various diameters and pitches. This selective thermal ALD process can thus enable finer gaps and pitches.

IV. Conclusion

This work has demonstrated a preliminary selective Co thermal ALD bonding process between horizontal Cu bonding pads. A thermal simulation benchmarked Co ALD bonds compared to conventional bonding technologies such as µ-bumps and hybrid bonds, demonstrating the potential thermal benefits of this bonding technology with a high thermal conductivity material surrounding the bonds. SEM, EDAX, and XPS were used to characterize the horizontal Cu pads separated by a 100 nm gap before and after deposition. Although 1% of Cu contamination on the insulator substrate is enough to activate Co growth, pre- and post-deposition treatments can be used to remove unwanted Co growth. This shows that using selective Co thermal ALD as a bonding process has the potential to aggressively shrink Cu I/O pitch to sub-micron.

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